A Standard-Cell-Based Neuro-Inspired Integrate-and-Fire ATC for Biological and Low-Frequency Signals

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***Abstract*—Continuous-time (CT) asynchronous data converters namely, ADCs and analog-to-time converters (ATCs), can be beneficial for certain types of applications, such as, processing of biological signals with sparse information. A particular case of these converters is the integrate-and-fire converter (IFC) that is inspired by the neural system. This paper presents a standard-cell-based (SCB) open-loop IFC circuit, designed and prototyped in a 130 nm CMOS standard process. It has a power dissipation of 59 μW and an energy *per* pulse of 18 pJ, which is one of the lowest energy *per* pulse consumption reported for IFC circuits, without requiring an external clock. The maximum pulse density (average firing-rate) is 3300 kHz. It is mostly digital, using only two additional on-chip integrating capacitors.**

***Index Terms*—ADC, analog-to-time converter (ATC), integrate-and-fire converter (IFC) circuit, Neuroelectronics, standard-cell-based (SCB), time encoding machine (TEM).**

I. Introduction

ASYNCHRONOUS CT ATCs and ADCs present interesting capabilities for certain applications, for example, those dealing with low frequency signals with sparse information. Biological signals such as electrocardiogram (ECG) or neuron signals (electrocorticogram (ECoG) - for brain-computer interfaces (BCIs), local field potentials (LFPs) or single neuron action potentials - for brain-machine interfaces (BMIs)) are potential examples. On the other hand, CT based ADCs have been the subject of increased interest in the last years, due to expected better performance with technology scaling-down, when compared to conventional ADCs. For certain cases, particularly for higher frequency input signals, as these topologies can take advantage of gate delay reduction and work at reduced voltage headroom [1], as they are single bit implementations. Asynchronous CT ATCs are a particular case of these types of samplers, where the analog input is converted into a time vector, indexed to the time of conversion. This is the case of an IFC circuit, it creates an amplitude-to-time conversion, having a stream of pulses as output. As it is asynchronous, the circuit only fires a pulse when the input signal time integration is above a defined threshold. This means that small variations in the input signal, that for certain applications do not contain relevant information, will not be converted, reducing the overall system power dissipation and creating a converted signal with lower data rate than in a common ADC. It is possible to reconstruct the input signal from the output pulse stream as shown in [2]–[4], or work in time domain, with the pulse output, doing pulse processing [5]–[12]. With the scaling down of CMOS technologies, digital cells perform better than more complex analog blocks and can work at reduced voltage headroom. This paper presents a SCB CT asynchronous ATC that does not require an external clock signal. It is an open-loop IFC, fully synthesizable and dynamic as each individual block can be powered off. As it operates asynchronously, having low power dissipation, and with pulse outputs with low data rates, it is a good solution for edge applications, such as low-power sensors analog frontend (AFE) interfaces in internet-of-things (IoT) applications.

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II. Asynchronous CT ATC and IFC Circuits

The IFC was originally developed as a neuron model, as it is inspired by the behavior of individual neurons. Carver Mead explored methods to relate electronic circuits and neuron modeling [13]. Since then IFC have evolved to have more versatility and lower power dissipation, [2], [14], [15].

Du Chen *et al.* developed a CMOS implementation of a biphasic IFC, as shown in Fig. 1, [3], with positive and negative thresholds and with refractory period control. That is an extension of a single-phase IFC, using a comparator [14], with input shifted by a common-mode (CM) voltage V_{mid} and with positive and negative firing thresholds, relative to this CM voltage. Rastogi [16] presents a new biphasic IFC circuit with refractory period control, using a starved inverter. Patil, *et al.*, [17] present a low power 10 MHz CT ADC that consists in an ATC with off-chip reconstruction of the original input signal from the output time series. It uses a comparator block that requires calibration, complex clocks, and offline time. It has a simple comparator block with four inverters that requires calibration every 2 ms, that lasts 1.5 μs, to set up the comparator threshold. This calibration scheme requires 3 clock signals. This increases system complexity due to the comparator choice. In the proposed asynchronous SCB IFC solution the comparator is based on a NAND latch, not requiring any calibration. Therefore, the sampler does not have offline time. Moreover, the system becomes simpler, by not requiring clocks or control signals. The authors in

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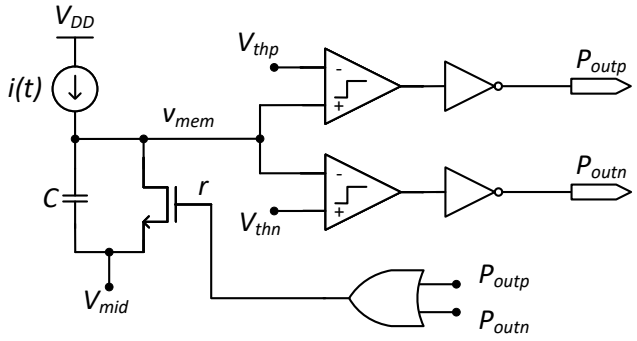

Fig. 1. Circuit schematic of a biphasic IFC as reported in [3].

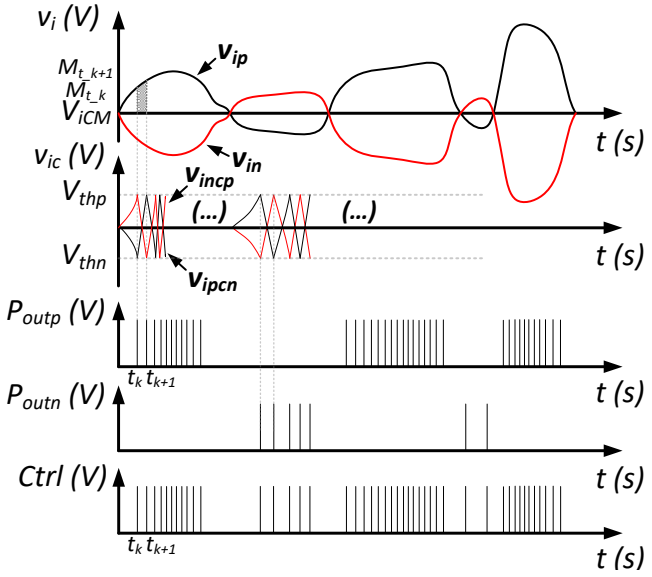

Fig. 2. Biphasic IFC input and pulse output and timing diagram of important signals for the proposed SCB IFC.

[18]–[22] present IFCs for neuromorphic applications, with a continuous decrease in energy *per* pulse consumption in more recent publications. A digital IFC neuron has been presented in [18], which is quite different from the proposed SCB IFC. It performs the neuron function by using digital logic and operations, while the proposed SCB IFC reproduces the analog IFC behavior, using digital blocks that perform in the analog and mixed-signal domains.

III. The Proposed Integrate-and-Fire Converter Circuits

The IFC integrates the input signal over time, generating a pulse when the integrated signal crosses the defined threshold. A pulse is generated when the area under the input signal curve is larger than a value k. Fig. 2 presents a representation of an input signal and the corresponding pulse outputs for a biphasic IFC, the area k is the trapezoidal grey area under the input signal. The number of output pulses, i.e., the pulse density, is proportional to the input signal amplitude and inversely proportional to its frequency. Fig. 3 presents the IFC block diagram (box in the figure bottom left corner), where K_I is the integration gain and q_e the quantization error, with a reset negative feedback path that corresponds to a return-to-zero, as in [23]. Hence, the IFC is a sampler that converts a continuous signal amplitude into time, with an injective 1-to-1 mapping, and, therefore, it has a defined reconstruction, under certain constraints [4]. The leaky IFC can be represented by (1) with the IFC sampler values defined recursively [4], [5]:

$$\int_{t_k+\tau}^{t_{k+1}} x(t)e^{\alpha(t-t_{k+1})}dt = q_k \tag{1}$$

where $q_k \in V_{thp}, V_{thn}$ the positive, or negative spiking threshold, respectively (relative to the amplifier input common-mode voltage (V_{iCM})), t_k and t_{k+1} are the occurrence timings of two successive pulses, τ is the refractory period, α is the leakage parameter, and $e^{\alpha(t-t_{k+1})}$ the integration leaky factor [5]. The inter-pulse interval (IPI) is defined as the time between two adjacent pulses, corresponding to the integrating time (2).

$$\mathrm{IPI}(t_{k+1}) = t_{k+1} - t_k \tag{2}$$

Equation (1) provides the relation between the IPI and the input signal. The number of output pulses, i.e., the pulse density, is proportional to the input signal amplitude and inversely proportional to its frequency. The proposed SCB open-loop biphasic IFC is shown in Fig. 3. It consists in an open-loop integrator with input cross switching and is composed of logic gates and switches. It has inverter-based amplifiers with enable and two double 3-port NAND latch comparators. Both blocks have enable inputs (*ENAmp* and *ENComp*) and they can be powered-off, independently, making this IFC version a fully-dynamic system. Since all blocks rely on custom sized standard-cells, the system is fully synthesizable, simply with the addition of two on-chip MIM integrating capacitors. As the input for this IFC circuit was chosen to be differential, it is possible to discharge the integrating capacitors through a simple input inversion, or cross-switching the input ports, as in a chopping amplifier. Although in this case there is no chopping after the amplifier outputs (in the analog domain) and there is only in the pulse outputs, to have a pulse in the correct output, positive or negative, even with cross-switched inputs, as described in [17]. When the integrated signal crosses the NAND latches internal thresholds, a pulse is generated and the amplifier inputs are cross switched, discharging the integrator capacitors. The SCB comparator inherent thresholds, together with C_f, define the resolution of the IFC circuit. The input switches are controlled by two comparators that are triggered by the integrated signal. The integration is reset by the lower and upper inner thresholds of the 3-port NAND latch. The reset path is similar to [17], using toggle flip-flops (TFFs) to retain the comparator last state, but has edge detectors to create the output pulses. The two inverters with inputs, v_{oncn} and v_{opcp}, are used only as load of the NAND latches. The input signal is integrated in capacitors C_f. For example, assuming that *Ctrl* is at high level, if v_{in} is negative relative to V_{iCM}, the amplifier output v_{ipcn} charges the top capacitor C_f, v_{incp}

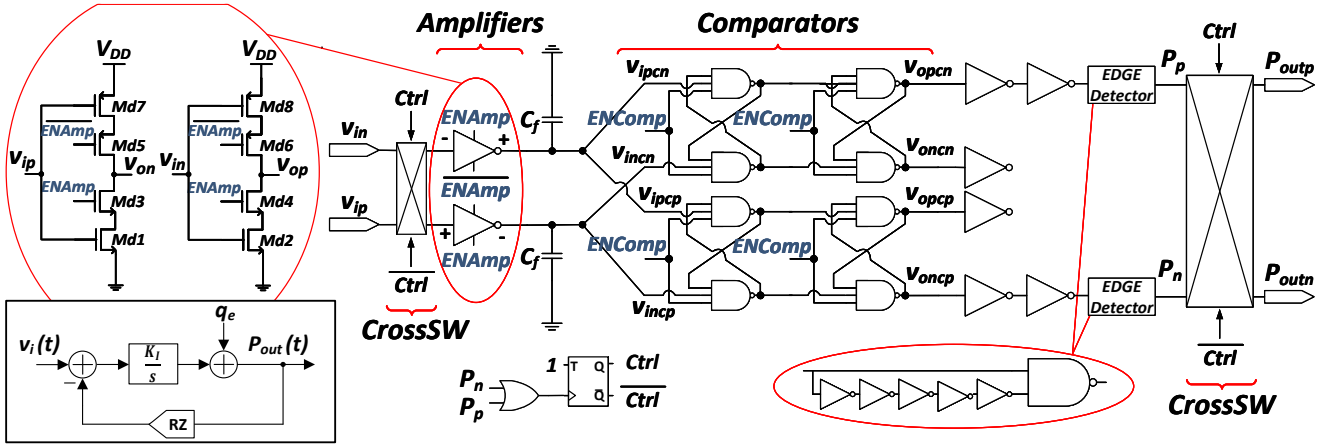

Fig. 3. SCB IFC circuit. Pulse outputs (P_{outp} and P_{outn}) drive TFFs, not shown. The double NAND latches are required to prevent metastability issues.

discharges the bottom capacitor C_f. When v_{ipcn} rises above the NAND internal threshold, the double NAND latch comparator output v_{opcn} passes to high creating a square wave after the top edge detector. This rapid square wave corresponds to a pulse in P_p and P_{outp}. Note that node v_{incp} is discharging and, therefore, v_{oncp} has low level output, and P_n and P_{outn} stay at low level. The positive output in P_p creates a transition in the TFF with $Ctrl$ outputs, lowering $Ctrl$, that switches both the inputs and outputs. As v_{in} is still negative and v_{ip} is positive, the top capacitor C_f is now discharging and the bottom one is charging. As v_{incp} voltage increases, when it passes the NAND latch internal threshold, the bottom double latch comparator passes v_{oncp} to high level and creates a pulse in P_n, and so another pulse in P_{outp}. As P_n passes to high level, the $Ctrl$ signals switch again due to the bottom TFF, making the inputs and outputs cross-switch again. For positive v_{in} the IFC creates pulses in P_{outn}. A fully-digital (SCB) IFC has been implemented with this topology that is quite different from the classic analog IFC. It benefits from being an open-loop approach. This reduces the Nyquist noise contribution and it improves the noise performance. The IFC has the input transistors (Md1,2 and Md7,8) in the active region and without velocity saturation, and the enable transistors (Md3-6) in the triode region. The expression of the dc gain in this case is given by (3).

$$A_{amplifier} \cong -(g_{m1,2}+g_{m7,8}) \times \\ [g_{m3,4}r_{ds3,4}r_{ds1,2} \| g_{m5,6}r_{ds5,6}r_{ds7,8}] \quad (3)$$

IV. Integrated Prototype Simulation and Measurement Results

Fig. 5 presents the layout of the SCB IFC circuits and also the die photo, in the red box in the bottom right, of the prototyped integrated circuit (IC) fabricated in a 1.2 V, 130 nm standard CMOS technology. The input signal reconstruction from the output pulse train can be achieved either by direct interpolation of the integration curve, or by more advanced methods, such as weighted low-pass kernel method for spiking neuron signals [2], [4]. From the triangular interpolation of the integration curve, the input signal information can be obtained from the IPI, (2), considering that the integration value k is constant. The SCB IFC can convert signals with a peak-to-peak amplitude from 1.6 mV to 28 mV and a frequency range of 2 Hz to 42 kHz The maximum pulse density (average firing-rate) is 3300 kHz. The inverter-based amplifier measured gain and bandwidth (BW) is approximately 27 dB and 8 kHz, respectively. Obtained from the differential magnitude response measurement for a -47 dBV input. The measured gain is in accordance with the theoretical gain calculated with (3), considering the operating point simulation results. Fig. 5 presents the measured inverter-based amplifier differential FFT for a 1 kHz, -60 dBV input. The SFDR is 53 dB. Fig. 4 presents the SCB IFC prototype measured pulse outputs, IPIs (2), and reconstructed input signal, considering triangular interpolation, for an input signal with 14 mV peak amplitude and frequency of 1 kHz. Measurements were made with amplifier and comparator enable voltages at V_{DD}, as well as close to the mid point voltage of each block, to test linearity. This measurement was obtained with $ENAmp = 465$ mV, $ENComp = 900$ mV, and $V_{iCM} = 478$ mV, instead of $V_{iCM} = 435$ mV (that is the amplifier inverter mid point voltage V_{Mid} for this measured chip, when $ENAmp = 900$ mV), because this provides better linearity. Due to the open loop configuration and inverter-based amplifier, the circuit is more sensitive to V_{iCM} and supply voltages when compared to closed loop implementations. The amplifier has maximum gain when $V_{iCM} = V_{Mid}$ and process, supply voltage, and temperature (PVT) simulation results with R+C+CC extraction show a V_{Mid} range of 425 mV to 435 mV, from fast fast to slow slow corners, respectively. Although the third harmonic is more than 61 dB below the fundamental frequency (Fig. 5), with -60 dBV input signal, the SCB IFC presents some crossover distortion. To further increase linearity, a Gm amplifier could be used instead of the inverter amplifier, as in [17]. However, the proposed architecture, based on a minimalist inverter-based amplifier (class B amplifier) and open-loop configuration achieves the required linearity while being fully synthesizable. The SCB IFC has a dynamic power

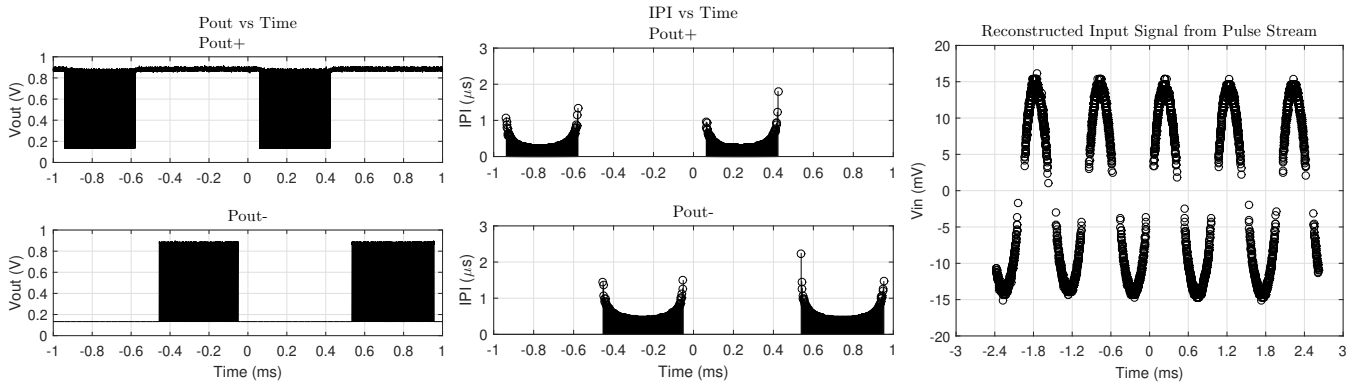

Fig. 4. SCB IFC measurement results: pulse outputs (left), IPI (middle), and reconstructed input signal from pulse outputs (right), for an input signal with a 14 mV peak amplitude and 1 kHz frequency. In this case, $ENAmp = 465$ mV and $V_{iCM} = 478$ mV, to have better linearity.

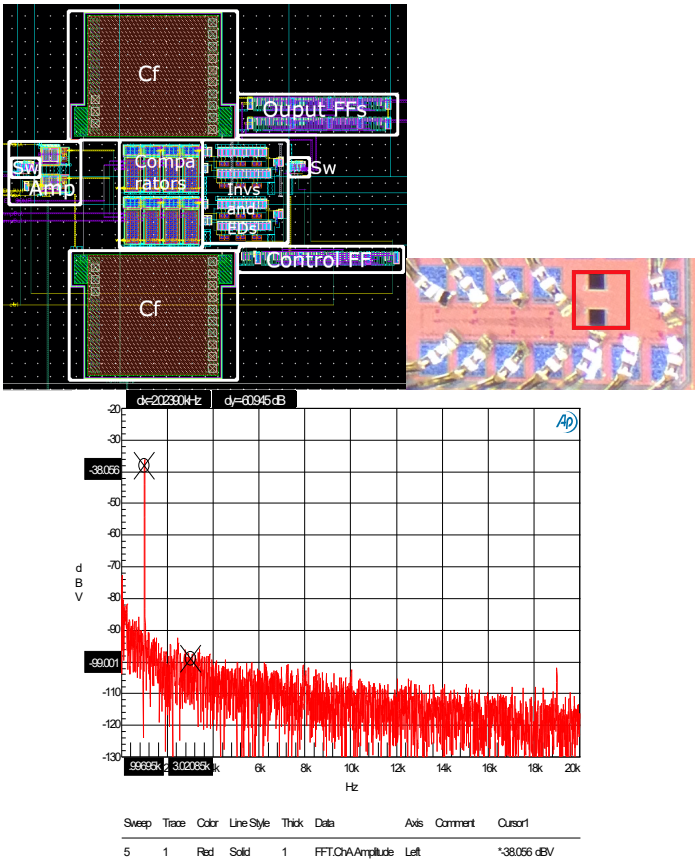

Fig. 5. Top: SCB IFC circuit layout in 130 nm CMOS technology, area 0.021 mm^2 and chip photo in the right (active area in red). Bottom: Inverter-based amplifier FFT, measured with an input signal of −60 dBV at 1 kHz.

dissipation of approximately 59 μW, from prototype measurements. Table I presents the prototype comparison SCB IFCs with the state-of-the-art. The proposed IFC is the first SCB and the only one that can be used standalone as an AFE in this comparison. [16] and the proposed IFC are the only biphasic IFCs in this comparison. The average firing-rate approximation of 3300 kHz for the proposed SCB IFC was obtained for

TABLE I
PROTOTYPE COMPARISON

Work	TCASI [20]	F.Neuro. [21]	TCASI [22]	NatureC. [19]	ISCAS [16]	**This Work**
Tech. (nm)	$22_{(a,b)}$	65	$28_{(b)}$	180	600	**130**
Supply (V)	0.8	0.2	0.2-1	1.8	5	**0.9**
Area (mm^2)	-	35×10^{-6}	13.3×10^{-6}	0.018	-	**0.021**
Power (μW)	-	1×10^{-4}	1.85×10^{-4}	27.3	1.2	**59**
Energy *per* Pulse (pJ)	1 @2.1 kHz	4×10^{-3}	0.43×10^{-3}	883 @30 Hz	10 @200 Hz	**18**
Avg. Firing-rate (kHz)	0.07	25	430	-	40	**3300**

(a) FDSOI (b) From simulation results, i.e., not prototyped.

an input signal with frequency of 1 kHz and 14 mV peak amplitude, Fig. 4. The energy *per* pulse was calculated for the presented average firing-rate, or stated otherwise in table I, considering $Energy-per-Pulse = \frac{Power}{Avg.\ Firing-rate}$.

V. CONCLUSIONS

A pseudo-differential voltage mode SCB IFC circuit with 0.9 V supply is presented in this paper. It was prototyped in a 1.2 V 130 nm CMOS standard process. It occupies an area of 0.021 mm^2 and it is the first of its kind. The SCB IFC is fully digital, dynamic, synthesizable and can be used as AFE in sensor-to-digital interfaces. It has a total power dissipation of 59 μW and an energy *per* pulse consumption of 18 pJ. This is one of the lowest energy *per* pulse consumption reported for IFC circuits. It represents a low power solution with low output data rates, that can be considered for biological implantation, or as an AFE for low frequency signals, as required in IoT.

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