A Standard-Cell-Based Neuro-Inspired Integrate-and-Fire Analog-to-time converter for Biological and Low-Frequency Signals - Comparison with Analog Version

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***Abstract*— Continuous-time asynchronous data converters namely, analog-to-digital converters and analog-to-time converters, can be beneficial for certain types of applications, such as, processing of biological signals with sparse information. A particular case of these converters is the integrate-and-fire converter (IFC) that is inspired by the neural system. If it is possible to develop a standard-cell-based (SCB) IFC circuit to perform well in advanced technology nodes, it will benefit from the simplicity of SCB circuit designs and can be implemented in widely available field-programmable gate arrays (FPGAs). This way, this paper proposes two IFC circuits designed and prototyped in a 130 nm CMOS standard process. The first is a novel SCB open-loop dynamic IFC. The latter, is a closed-loop analog IFC with conventional blocks. This paper presents a through comparison between the two IFC circuits. They have a power dissipation of 59 μW and 53 μW, and an energy *per* pulse of 18 pJ and 1060 pJ, SCB and analog IFC, respectively. The SCB IFC has one of the lowest energy *per* pulse consumption reported for IFC circuits. The analog IFC, being fully differential, is to our knowledge the first of its kind. Moreover, they do not require an external clock. They can convert signals with a peak-to-peak amplitude from 1.6 mV to 28 mV and 0.6 mV to 2.4 mV, and a frequency range of 2 Hz to 42 kHz and 10 Hz to 4 kHz, SCB and analog IFC, respectively. Presenting low normalized RMS conversion plus reconstruction errors, below 5.2 %. The maximum pulse density (average firing-rate) is 3300 kHz, for the SCB and 50 kHz, for the analog IFC.**

***Index Terms*— ADC, analog-to-time converter, integrate-and-fire converter, ECG, neuroelectronics, standard-cell-based, time encoding machine.**

I. Introduction

ASYNCHRONOUS continuous-time (CT) analog-to-time converters (ATCs) and analog-to-digital converters (ADCs) present interesting capabilities for certain applications, for example, those dealing with low frequency signals with sparse information. Biological signals such as electrocardiogram (ECG) or neuron signals (electrocorticogram (ECoG) - for brain-computer interfaces (BCIs), local field potentials (LFPs) or single neuron action potentials - for brain-machine interfaces (BMIs)) are potential examples. On the other hand, CT based ADCs have been the subject of increased interest in the last years, due to expected better performance with technology scaling-down, when compared to conventional ADCs. For certain cases, particularly for higher frequency input signals as these topologies can take advantage of gate delay reduction and work at reduced voltage headroom [1], as they are single bit implementations. Asynchronous CT ATCs are a particular case of these types of samplers, where the analog input is converted into a time vector, indexed to the time of conversion. This is the case of an integrate-and-fire converter (IFC) circuit, it creates an amplitude-to-time conversion, having a stream of pulses as output. As it is asynchronous, the circuit only fires a pulse when the input signal time integration is above a defined threshold. This means that small variations in the input signal, that for certain applications do not contain relevant information, will not be converted, reducing the overall system power dissipation and creating a converted signal with lower data rate than in a common ADC. It is possible to reconstruct the input signal from the output pulse stream as shown in [2]–[4], or work in time domain, with the pulse output, doing pulse processing [5]–[12].

With the scaling down of CMOS technologies, digital cells perform better than more complex analog blocks and can work at reduced voltage headroom. If it is possible to develop a standard-cell-based (SCB) IFC circuit to perform well in advanced technology nodes, that can be synthesizable, it will also benefit from the simplicity of SCB circuit designs and can be implemented in widely available field-programmable gate arrays (FPGAs), without requiring dedicated integrated circuit (IC) circuitry. This paper verifies this hypothesis and confirms if a SCB IFC circuit would have lower energy consumption, higher dynamic range and versatility than a conventional IFC circuit with analog blocks. This paper presents a SCB CT asynchronous ATC, previously published in [13] and compares it with a biphasic fully differential IFC circuit, both designed and prototyped in a 130 nm CMOS standard process. The

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first is an open-loop IFC, fully synthesizable and dynamic as each individual block can be powered off. The latter, is a closed-loop analog IFC with conventional blocks, although not sacrificing either the chip area or power. Both have on chip capacitors. As they operate asynchronously, having low power dissipation, and with pulse outputs with low data rates, they are good solutions for edge applications, such as low-power sensors analog frontend (AFE) interfaces in internet-of-things (IoT) applications.

This paper is organized as follows. Section II presents the state-of-the-art of IFC and similar ATCs. Section III presents the IFC neuron model, the sampler details, and the design of the corresponding circuits, and section IV shows the simulation and the experimental results, and comparison between SCB and analog versions. Conclusions are drawn in section V.

II. Asynchronous CT ATC and IFC Circuits

The IFC was originally developed as a neuron model, as it is inspired by the behavior of individual neurons. Carver Mead explored methods to relate electronic circuits and neuron modeling [14], Fig. 1 (a). His original spiking neuron hardware model consists of an axon-hillock circuit with a capacitor voltage-divider with the addition of a self-reset. This way it can recover to the initial condition and fire more than once. The axon-hillock circuit consists of an input capacitor plus two inverters with a positive-feedback through an integrating capacitor. This implementation has a fixed firing threshold that varies with process, supply voltage, and temperature (PVT). Moreover, if the input is close to the inverters mid point, both PMOS and NMOS inverter transistors are ON, increasing the power dissipation due to a short-circuit current. It also has a fixed refractory period. Sarpeshkar, Watts, and Mead present in [15] their sodium-potassium neuron circuit with an operational amplifier (OP-AMP), used as a comparator, to have variable firing threshold, Fig. 1 (b). The transistors directly translate the neuron ionic behavior. This neuron has both positive and negative feedback, variable firing threshold and pulse width, and refractory period control. To have better power management than [14] spiking neuron, [16] developed a current-feedback latch that reduces the short-circuit power dissipation in the input stage, Fig. 1 (c). Since then IFC have evolved to have more versatility and lower power dissipation [2], [17], [18], Fig. 1 (d) and (e).

Du Chen *et al.* [3], Fig. 2, and Rastogi *et al.* [19] present two different biphasic IFC circuits. Patil, *et al.* [20] present a low power 10 MHz CT ADC that consists in an ATC with off-chip reconstruction of the original input signal from the output time series. The authors in [21]–[25] present IFCs for neuromorphic applications, with a continuous decrease in energy *per* pulse consumption in more recent publications. A digital IFC neuron has been presented in [21] that works in digital domain.

An IFC differential solution is better than having two IFCs, one for each differential input, because it has less mismatch between the two input branches. It also provides better balancing, as the bias current increases in one input branch and decreases in the other. This is particularly important in the comparator stage and improves linearity. Although, nonlinearity can be used as an advantage in IFC systems, as shown in [26]. In that work a signal-to-noise ratio (SNR) reduction from modulation of rate coded coupled neuron population network is shown. This allows the uses of unsynchronized, slower, and unprecise individual IFC neurons to process higher frequency signals, similar to what is believed to occur in brain processing. Two IFCs in parallel could be a possible alternative, but there would be a mismatch between transistors and firing thresholds. The work in [27] presents a new IFC system with delta and pulse frequency modulations that has an inbuilt AFE with an low noise amplifier (LNA), being different than the proposed IFCs in which the neuron/IFC is in itself an AFE. The work [28] presents an assynchronous biphasic delta modulator with adaptive thresholding capable of being used as an AFE. It presents interesting characteristics to be used as a permanent online system, the adaptive thresholding is used to reduce sensibility to baseline and background signals, and noise. If the threshold adaptation is too prominent, the input reconstruction will not be possible, unless the thresholds are also recorded. But even in such a case, without recording the thresholds, the system can perform well doing time domain feature extraction.

III. The Proposed integrate-and-fire converter circuits

The IFC integrates the input signal over time, generating a pulse when the integrated signal crosses the defined threshold. A pulse is generated when the area under the input signal curve is larger than a value ka. Fig. 3 presents a representation of an input signal and the corresponding pulse outputs for a biphasic IFC, the area ka is the trapezoidal grey area under the input signal. Fig. 4 presents the IFC block diagram, with an integration block, where K_I is the integration gain, a comparison block which adds the quantization error q_e, a reset negative feedback path that resets the integration by discharging the integration capacitor. This reset path corresponds to a return-to-zero, as in [29]. This structure is similar to a delta modulator, in fact the IFC is a special case of an asynchronous first order $\Sigma\Delta$ modulator [30], [31]. With dc input, the IFC fires pulses, as the dc voltage charges the integration capacitors. Hence, in the theoretical model, the IFC is a sampler that converts a continuous signal amplitude into time, with an injective 1-to-1 mapping, and, therefore, it has a defined reconstruction, under certain constraints [4]. The leaky IFC can be represented by (1) with the IFC sampler values defined recursively [4], [5]:

$$\int_{t_k+\tau}^{t_{k+1}} x(t)e^{\alpha(t-t_{k+1})}dt = q_k \tag{1}$$

where $q_k \in V_{thp}, V_{thn}$ the positive, or negative spiking threshold, respectively (relative to the amplifier input common-mode voltage (V_{iCM})), t_k and t_{k+1} are the occurrence timings of two successive pulses, τ is the refractory period, α is the leakage parameter, and $e^{\alpha(t-t_{k+1})}$ the integration leaky factor [5]. The inter-pulse interval (IPI) is defined as the time between two adjacent pulses, corresponding to the integrating time (2).

$$\mathrm{IPI}(t_{k+1}) = t_{k+1} - t_k \tag{2}$$

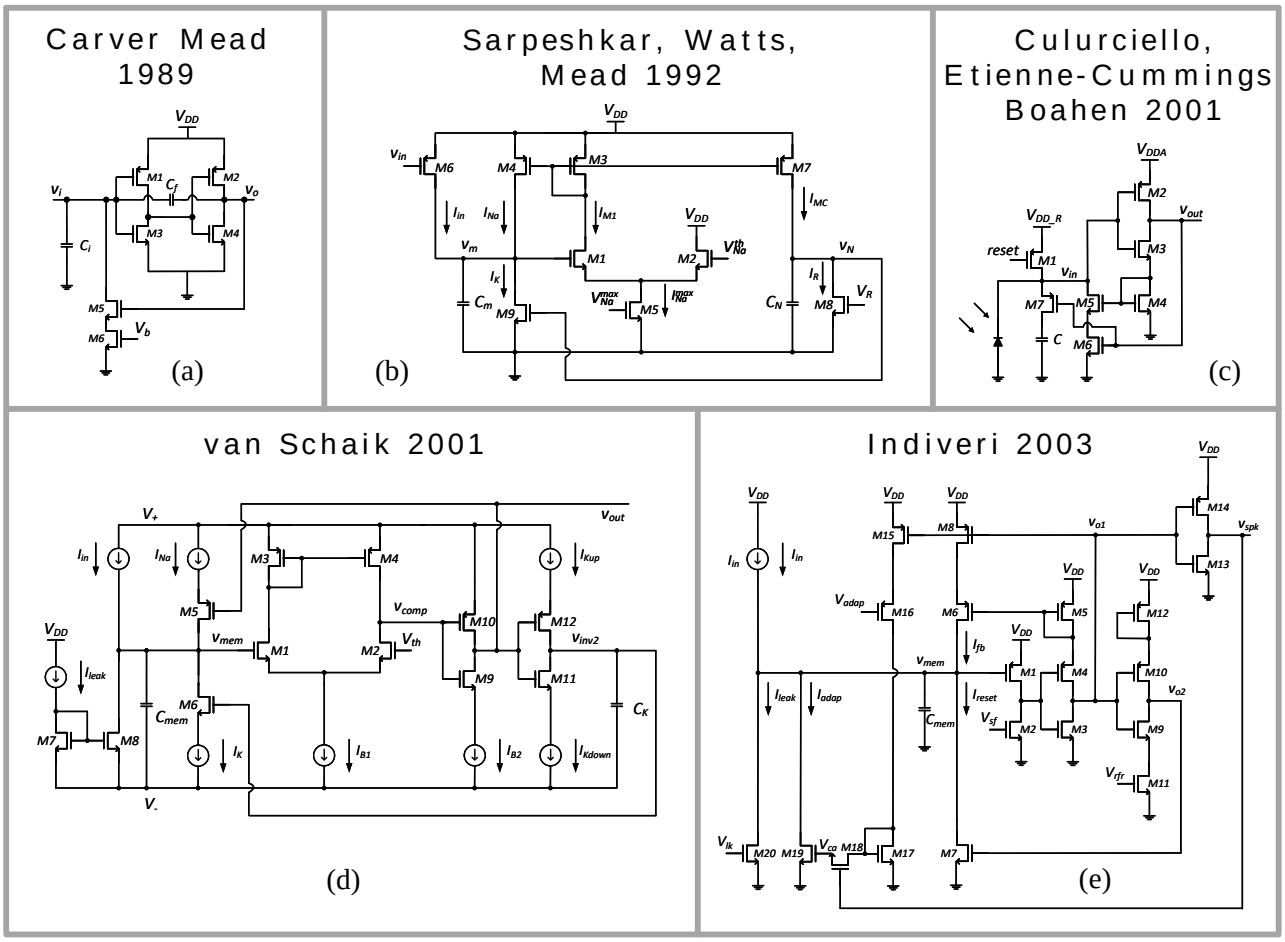

Fig. 1. IFC circuits state-of-the-art (SoA) evolution [14]–[18].

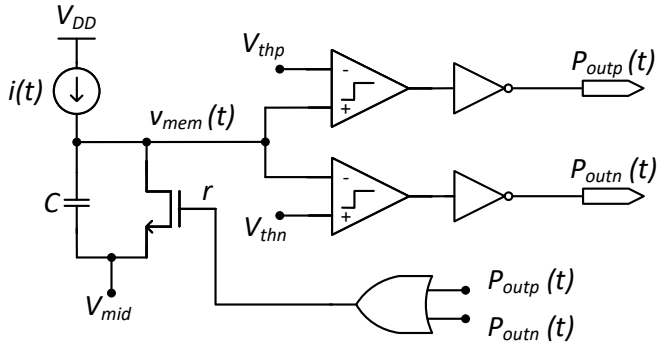

Fig. 2. Circuit schematic of a biphasic IFC as reported in [3], modified from [13].

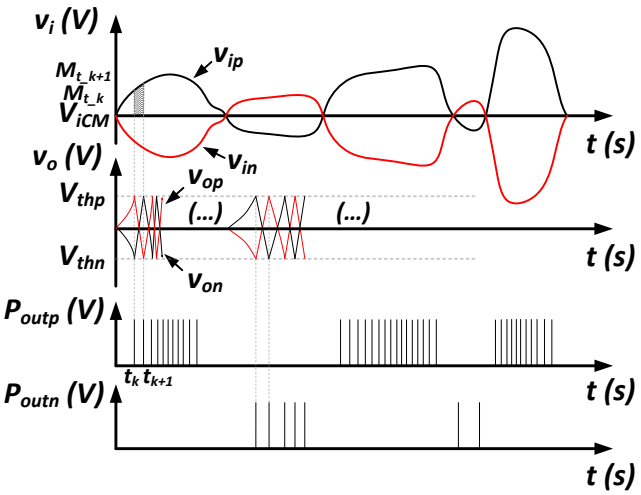

Fig. 3. Biphasic IFC input and pulse output and timing diagram of important signals, modified from [13].

Equation (1) provides the relation between the IPI and the input signal.

The proposed SCB open-loop biphasic IFC is shown in Fig. 5. It consists in an open-loop integrator with input cross switching and is composed of logic gates and switches. The circuit is described in detail in [13]. When the integrated signal crosses the NAND latches internal thresholds, a pulse is generated and the amplifier inputs are cross switched, discharging the integrator capacitors. Fig. 3 presents the timing diagram with important signals for both IFC circuits, v_{ic} is the comparator input voltage. In the analog IFC circuit version v_{op} and v_{on} are equivalent to v_{ipcn} and v_{incp}, respectively, in the SCB version. Table I summarizes the transistor dimensions of the inverter based amplifier and comparators (Mdc1-3 and Mdc4-6 are the NAND3 NMOS and PMOS transistors,

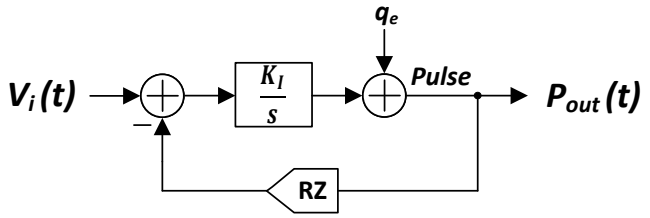

Fig. 4. Simplified IFC block diagram, modified from [13].

respectively). All dimensions presented in this paper are in a 1.2 V 130 nm CMOS standard process.

The analog IFC circuit is presented in Fig. 6. The proposed analog IFC has been implemented with conventional blocks. It comprises: a two-stage Miller compensated differential operational transconductance amplifier (OTA) with nulling resistor and an output common mode circuitry, differential comparators with dynamic biasing - power off capability, a NAND based edge detector, and a bootstrap circuit for the reset signal. As it is biphasic, there are two comparators, one for each threshold condition. Each comparator produces a pulse output (positive or negative pulse output). The pulse outputs control the transmission gates that reset C_f.

The amplifier of the integrator is a two-stage Miller-compensated differential OTA, Fig. 7, with 73 dB gain, 4 kHz bandwidth, and 14 MHz unity gain bandwidth with 1 µA PMOS polarization, dissipating 42.2 µW. With a phase-margin of 69 degrees. This OTA topology has been chosen due to the requirements of high-gain and wide output swing, larger than 150 mV for each branch, so output swing $v_{op} - v_{on} > 300$ mV.

The OTA output common-mode (CM) is adjusted with a common-mode feedback (CMFB) circuit, shown in Fig. 8, through voltage V_{bn} at the gate of M1-2 (NMOS active loads). The CMFB circuit presents good linearity as it replicates the OTA PMOS input differential pair and its load. The PMOS input pair and the second stage common sources were designed to operate in the subthreshold region to provide the maximum g_m/I_D ratio. The input pair and second stage common source transistors are in subthreshold region and remaining transistors are in the active region (with the exception of M20-21, that are in the triode region).

Tables II and III present the OTA and its CM transistors dimensions, respectively. Table IV presents the passive components values used in the OTA and integrator. All capacitors are of the type metal-insulator-metal (MIM).

The two comparators are identical, presented in Fig. 9, having 3.3 µW power dissipation each. The comparators output inverters are current starved inverters, with a tail NMOS with gate voltage V_{refrac}, that sets the refractory component, as in [32, p. 44]. The current starved inverter delay element

TABLE I
INVERTER BASED AMPLIFIER AND LATCH COMPARATORS NAND3 TRANSISTORS DIMENSIONS.

Transistor	Md1-4	Md5-8	Mdc1-3	Mdc4-6
W (μm)	2.8	8.4	12	2.4
L (μm)	0.36	0.36	1.2	1.2

TABLE II
OTA TRANSISTORS DIMENSIONS

Transistor	M1,2	M3,4	M5	M6,8	M7,9	M10
W (μm)	6	36	30	45	18	3
L (μm)	1	0.3	1	1	0.3	1

was proposed in [33]. The comparator has a replica bias circuit (RBC) to set the voltage in the crossed pair, before the output inverters. The RBC is a copy of one of the comparator branches with a feedback-loop with a simple single-ended single stage diode tied amplifier to set the desired voltage, Fig. 9. The comparator is dynamically biased, as [32, p. 57], having a close to power off capability, through the NMOS tail transistors Mc7a and Mc8a with gate voltage controlled by the comparator input signal. Considering there is no mismatch between the tail transistors, the comparator "turns ON" - has enough bias current with Mc7 out of the triode region and in the beginning of the saturation region ($V_{DSMC7} > V_{bn} - V_{T7}$) and Mc7a not in the subthreshold region, only when the comparator input signal is above approximately $V_{DSMC7} + V_{thMC7a}$, and the same for Mc8,a. Table V presents the comparators transistor dimensions.

TABLE III
OTA CMFB TRANSISTORS DIMENSIONS

Transistor	M11,12	M13	M14	M15-18	M19	M20,21
W (μm)	2	5	1	3	1	5
L (μm)	1	1	1	2	1	1

TABLE IV
PASSIVE COMPONENTS VALUES

Component	R_i (kΩ)	C_f (pF)	$R_{1,2}$ (kΩ)	$C_{1,2}$ (pF)
Value	268	2.04	5.5	1.04

TABLE V
COMPARATOR TRANSISTORS DIMENSIONS

Transistor	Mc1-6	Mc7-9a	Mc10-12
W (μm)	1.96	6	1.75
L (μm)	0.66	1	3.3

Mc13-15	Mc16-19	Mc20,21
1.4	0.64	1.92
3.3	1	1

In the analog IFC version, to discharge the C_f capacitor plates to the OTA input and output common mode it is required that the reset signal controls very large transmission gates, or with unreasonable multiplier. For this reason a bootstrap circuit, as presented in [34, Fig. 1], and [35], was used in the reset signal before it drives NMOS transistor in the transmission gate. In both versions, an edge detector circuit is required to generate a pulse because the comparators digital output stays at V_{DD} if one of the previous firing conditions is met. This way the edge detector creates a pulse with a width set by its delay cells, whenever the comparator output goes high. This pulse resets the integrating capacitor C_f, making again the comparator change to its low output state.

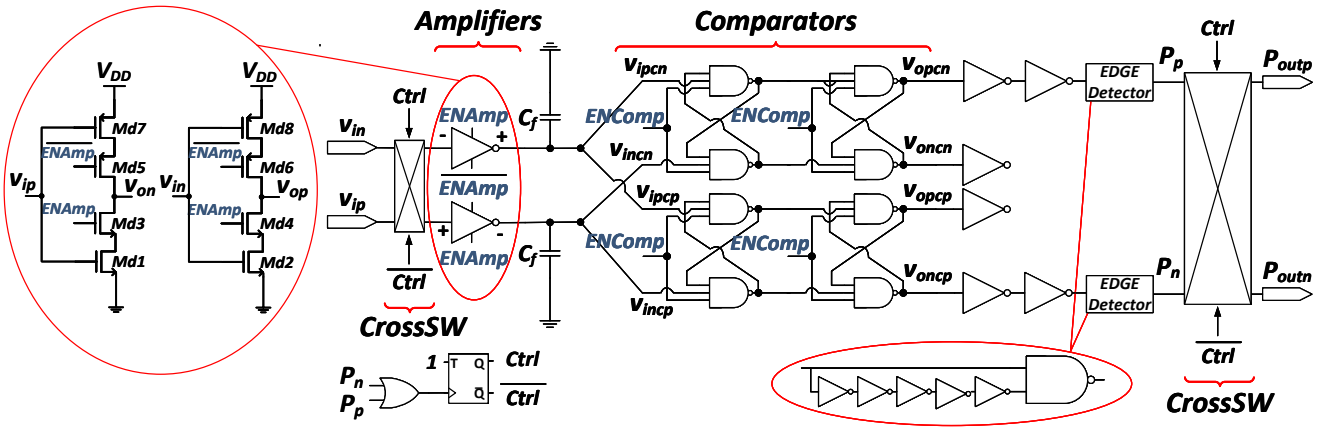

Fig. 5. SCB IFC circuit. Pulse outputs (P_{outp} and P_{outn}) drive TFFs, not shown. The double NAND latches are required to prevent metastability issues, modified from [13].

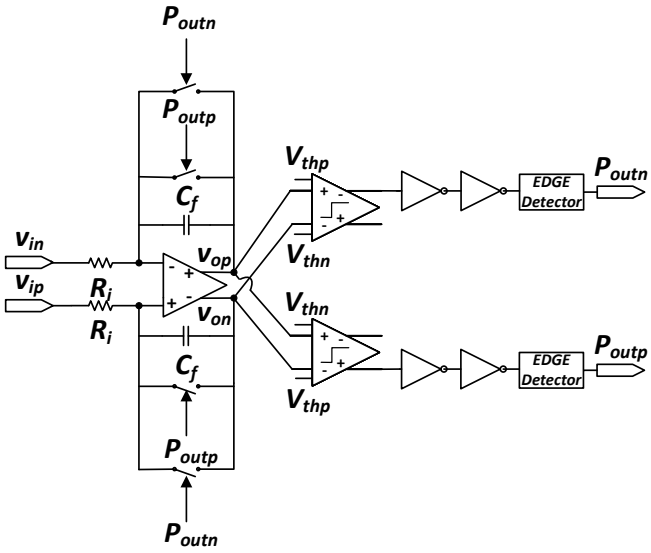

Fig. 6. Analog IFC circuit. Switches are transmission gates with bootstrapped NMOS and Pouts drive TFFs, both not shown.

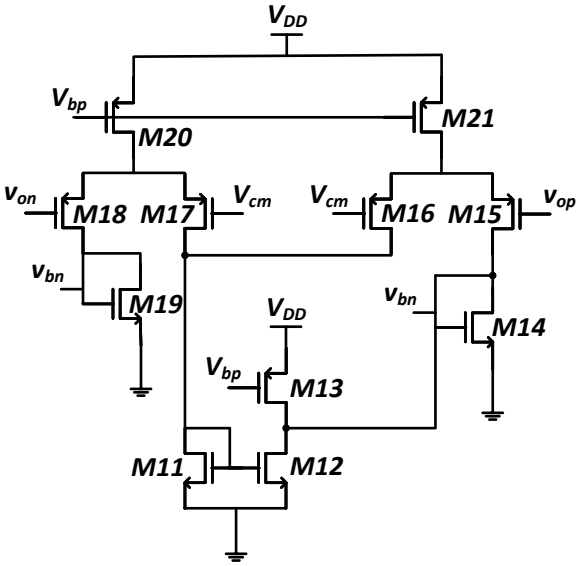

Fig. 8. The CT CMFB circuit used in the OTA.

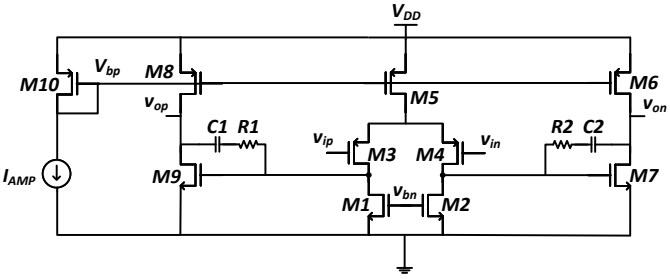

Fig. 7. Analog IFC two-stage Miller-compensated OTA circuit.

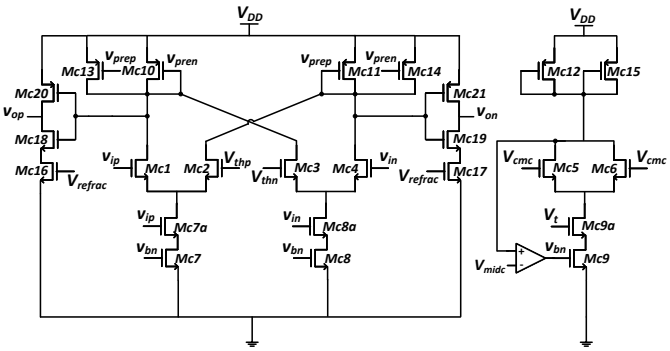

Fig. 9. Analog IFC fully differential comparator circuit with dynamic biasing through MC7a and 8a, plus RBC.

IV. Integrated Prototype Simulation and Measurement Results

Fig. 10 presents the layout and die photo of the analog prototyped IFC circuit. The layout of the SCB IFC circuit and also the die photo is presented in [13].

The input signal reconstruction from the output pulse train can be achieved either by direct interpolation of the integration curve, or by more advanced methods, such as weighted low-pass kernel method for spiking neuron signals [2], [4]. All reconstruction methods present a reconstruction error. The

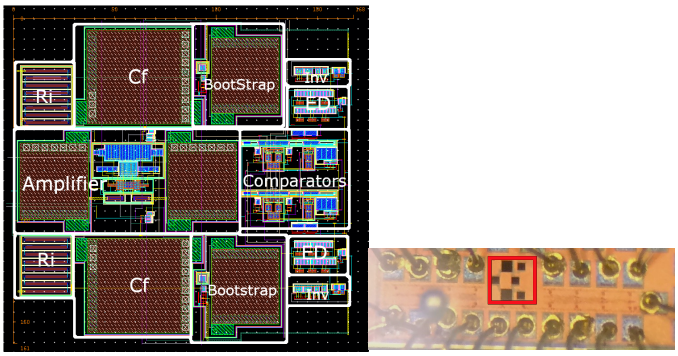

Fig. 10. Analog IFC circuit layout (left) and prototyped circuit (right, active area in red) in CMOS 130 nm, area 0.027 mm^2. Label ED stands for edge detector.

work in [4] proved that it is always possible to approximately reconstruct a bandlimited input signal from the output pulse train under certain constraints and the reconstruction error is bounded by the IFC firing threshold. From the triangular interpolation of the integration curve, the input signal information can be obtained from the IPI, (2), considering that the integration value ka is constant. The accuracy of the IFC pulse output measurement should be high, to minimize the error in determining the rise and fall timings of the pulse outputs that are the square wave outputs of the TFFs. The accuracy of this measurement introduces an error in the IPI calculation and so in the input signal reconstruction. The prototype measurements were made with a Rohde & Schwarz (R&S) RTO 1022 2 GHz, 10 GSa/s, oscilloscope that is capable of clearly measuring the fast transitions with high resolution, using passive probes, as R&S RT-ZP10 500 MHz, or the high bandwidth (BW) single ended active probes R&S RT-ZS30 2 GHz. All measurements have been made with the R&S active probes. The low amplitude input signals were generated with an Audio-Precision ATS-2 audio test system. The inverter amplifier fast-Fourier-transform (FFT), presented in [13] and Bode plot, not shown, were measured with the ATS-2. Simulations and layout were run in Cadence software and results were obtained with layout extraction.

The reconstruction algorithm consists in the following steps:

1) The prototypes pulse train outputs (square wave outputs of the TFF) are recorded with the RTO oscilloscope.
2) A software algorithm detects the transitions in the square waves and stores in a time series: the time of occurrence of each transition and the time difference to the previous transition - the IPI, (2). Note that each transition corresponds to an output pulse.
3) Considering that the integration value ka is constant, ka is calculated for a certain measurement by equation $ka = v_{inp}\,\mathrm{IPI}_{min}$, where v_{inp} is the input peak voltage and IPI_{min} the minimum IPI that occurs at the input voltage peak.
4) The input wave is reconstructed calculating the input amplitude value for each IPI, considering equation $v_{in}(t_{k+1}) = \frac{ka}{\mathrm{IPI}(t_{k+1})}$, t_{k+1} is the time of occurrence of the second output pulse, that corresponds to the input signal time.

The SCB IFC can convert signals with a peak-to-peak amplitude from 1.6 mV to 28 mV and a frequency range of 2 Hz to 42 kHz. The maximum pulse density (average firing-rate) is 3300 kHz. Simulations and measurements with different sinusoidal inputs were performed to measure the firing-rate, the input BW, minimum and maximum input amplitude, and power dissipation of each IFC circuit. Fig. 11 presents simulation results for the SCB IFC IC prototype, the IPIs and corresponding reconstructed input signal from pulse outputs, for an input signal with 11 mV peak amplitude and frequency of 100 Hz. The amplifier and comparator enable voltages were set to V_{DD} level, $ENAmp = ENComp = 900$ mV. The input signal CM voltage is $V_{iCM} = 427$ mV, as it is the inverter amplifier mid point, V_{Mid}, with amplifier enable voltage at V_{DD}. The IPIs are obtained through step 2 of the reconstruction algorithm, described previously, and the reconstruction curves are obtained considering steps 3 and 4. Fig. 12 presents the SCB IFC prototype measured IPIs (2), calculated from the measured pulse outputs, that were presented in [13], and reconstructed input signal, considering again triangular interpolation, for an input signal with 14 mV peak amplitude and frequency of 1 kHz. Fig. 12 presents the reconstructed signal with the best linearity from the SCB IFC measurements. The SCB IFC has a dynamic power dissipation of approximately 59 μW, from prototype measurements. Fig. 13 presents the analog IFC

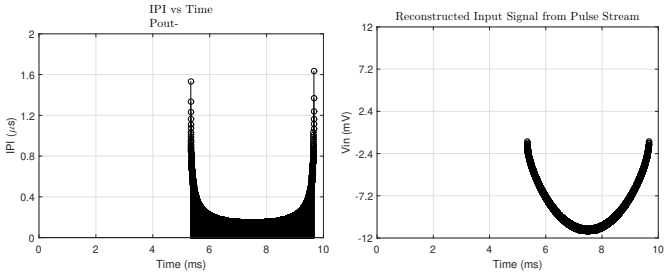

Fig. 11. SCB IFC version simulation results, IPI (left) and reconstructed signal from pulse outputs (right), for input signal with 11 mV peak amplitude and 100 Hz. $ENAmp = ENComp = 900$ mV, $V_{iCM} = 427$ mV. Only P_{outn} side.

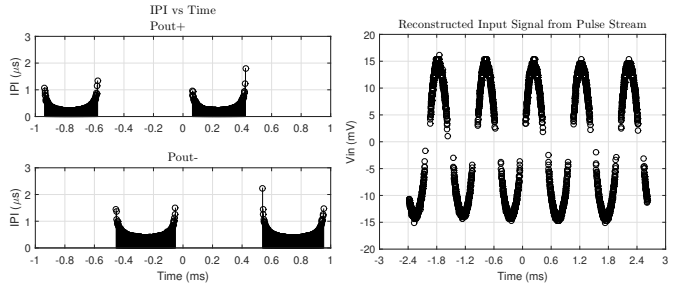

Fig. 12. SCB IFC measurement results: IPI (left), and reconstructed input signal from pulse outputs (right), for an input signal with a 14 mV peak amplitude and 1 kHz frequency. In this case, $ENAmp = 465$ mV and $V_{iCM} = 478$ mV, to have better linearity, modified from [13].

simulation results after layout extraction (C+CC and R+C+CC extraction type): IPI and reconstructed input signal from pulse outputs for two different differential sinusoidal input signals. The input CM is $V_{iCM} = 400$ mV and the amplifier output CM is $V_{oCM} = 500$ mV. The comparator thresholds were set as $V_{thn} = 400$ mV and $V_{thp} = 600$ mV. The minimum IPI for

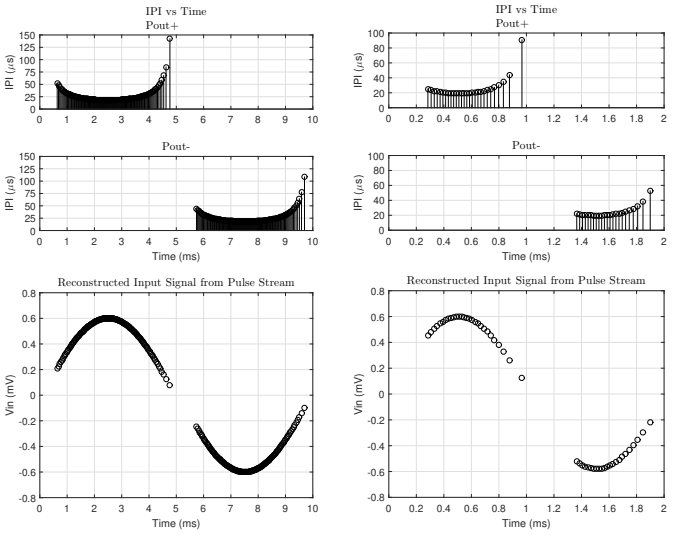

Fig. 13. Analog IFC simulation results after layout extraction (C+CC extraction left, R+C+CC right). The top row presents the IPI and the bottom row the reconstructed input sine wave from pulse outputs for different input signals with peak amplitude and frequency of: 600 μV and 100 Hz (left), 600 μV and 500 Hz (right).

1 mV amplitude and 1 kHz input is approximately 11 µs, for 10 mV and 1 kHz input is approximately 1.3 µs, and for 600 µV and 500 Hz input is approximately 18 µs, as can be seen in Fig. 13. Fig. 13 shows that for a fixed input amplitude the IPI is inversely proportional to the input frequency. Fig. 14 presents the measured IPI and respective reconstruction for an input signal with 600 µV peak amplitude and 100 Hz. The analog IFC circuit has a power dissipation of approximately 53 µW obtained in simulation after R+C+CC layout extraction and in measurement, with a 1 µA biasing current in the OTA and in each comparator. The number of output pulses, i.e., the pulse density, is proportional to the input signal amplitude and inversely proportional to the input signal frequency, as can be seen in Fig. 13. On the other hand, the firing-rate is proportional to the input signal amplitude and frequency. The maximum firing-rate as a function of input signal frequency and amplitude is presented for both IFC in Fig. 15 and Fig. 16. At high input amplitude and frequency the SCB IFC saturates and presents a nonlinearity that makes the firing-rate drop substantially. Note that the input peak amplitude is already above 14 mV that is considered the linear input range. The comparators voltage thresholds V_{th} define the resolution of the IFC circuit together with C value, in the case of the described analog IFC version, Fig. 2, and R_i and C_f values, in the case of the proposed analog IFC version, Fig. 6. However, only C_f and the SCB comparator inherent thresholds set the resolution, in the case of our SCB IFC version presented in [13], Fig. 5.

Simulations were run with an ECG input signal to verify the IFC circuit behavior when presented with a biological signal with sparse information. Fig. 17 presents the analog IFC simulation results after R+C+CC layout extraction for an accelerated ECG input signal. The ECG signal is from the PhysioNet ECG-ID database [36], [37] (Person 1, recording 1), the signal has the original time and amplitude divided by 100. A differential input with adjusted CM, $V_{iCM} = 400$ mV was created from this ECG signal and used as the analog IFC input. The positive and negative pulse outputs relative to the positive and negative portion of the ECG signal were used to calculate the respective IPI and then make the reconstruction of the ECG signal, both presented in Fig. 17. The reconstructed signal in Fig. 17 shows that the analog IFC is capable of processing ECG signals preserving the QRS complex timing and amplitude information.

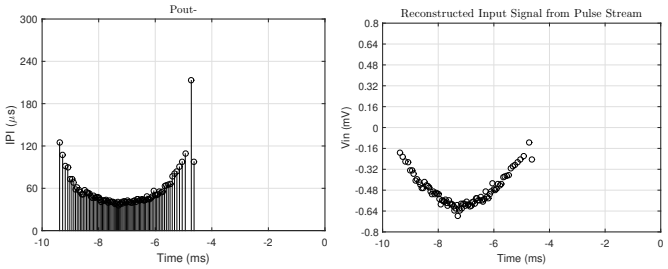

Fig. 14. Analog IFC prototype measurement, IPI (left) and reconstructed signal from pulse output (right), for input signal with 600 µV peak amplitude and 100 Hz. Only P_{outn} side.

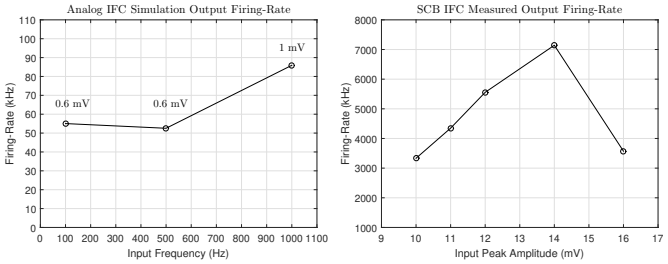

Fig. 15. Analog IFC Simulation output firing-rate (left), input peak amplitude in the data points label, and SCB IFC prototype firing-rate measurement (right) for an input signal frequency of 100 Hz.

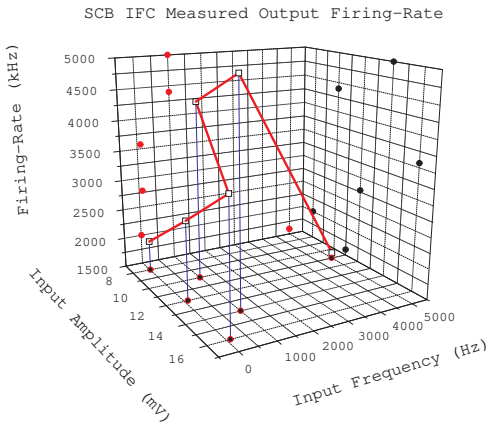

Fig. 16. SCB IFC prototype output firing-rate measurement, varying the input signal peak amplitude and frequency.

The conversion plus reconstruction error (conversion and reconstruction errors together) was calculated with the normalized mean absolute error (NMAE) and normalized root mean square error (NRMSE), considering a similar definition

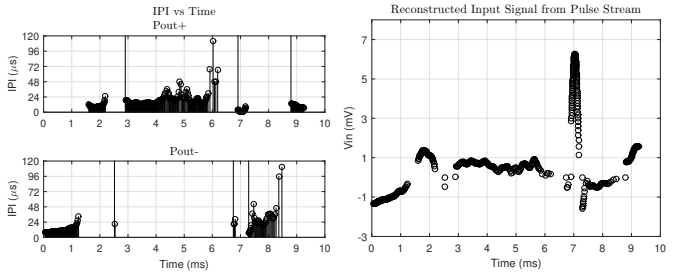

Fig. 17. Analog IFC version ECG simulation results: IPI (left) and reconstructed input signal from pulse outputs (right), for accelerated ECG input signal (R+C+CC extraction). PhysioNet ECG-ID database ECG [36], [37], with time and amplitude divided by 100. Differential input with adjusted CM, $V_{iCM} = 400$ mV.

to the one in work [38]:

$$\text{NMAE} = \frac{\|V_i - V_{iR}\|_1 / N}{max(V_{iR}) - min(V_{iR})} \times 100\% \quad (3)$$

$$\text{NRMSE} = \frac{\|V_i - V_{iR}\|_2}{\|V_{iR} - < V_{iR} >\|_2} \times 100\% \quad (4)$$

where V_i is the IFC input signal magnitude vector, meaning a vector with the input signal magnitudes at the time the second and consequent output pulses were generated, t_{k+1} in $\text{IPI}(t_{k+1})$, V_{iR} the reconstructed input signal magnitude vector with reconstructed input signal magnitude at the same time t_{k+1}, for each row, and N the number of points in V_i. The errors are presented in Table VI. The sine wave NRMSE is approximately 20 and 3 times smaller than the one presented for a quadratic chirp in [39] (4.4 %), for the SCB and analog IFC, respectively. The NRMSE for analog IFC reconstructed ECG is approximately 5 times smaller than the one in [39] (26.1 %), but at the cost of approximately 11 and 4 times more power dissipation for the ECG and quadratic chirp conversion, respectively. On the other hand, our reconstruction is much simpler, as we do not use polynomial interpolation, as in [39], which increases reconstruction complexity and power dissipation in the reconstruction phase. Fig. 18 presents the NMAE and NRMSE for the analog IFC *versus* input signal frequency. It represents the conversion plus reconstruction errors for the IFC curve in Fig. 15 (left). The SCB IFC with measured pulse outputs for 11 mA input signal peak amplitude and 5 kHz frequency (the lower point in Fig. 16 that is in the nonlinear conversion region) has conversion plus reconstruction NMAE and NRMSE of 3.1 % and 0.88 %, respectively. Table VII compares the proposed IFCs NMAE and NRMSE with the CT asynchronous sparse input signal SoA for different applications, platforms, and biological signals. The proposed IFCs have NMAE and NRMSE conversion plus reconstruction errors in line, or lower than the other works presented here.

The comparison between the proposed analog and SCB IFCs [13] is presented in Table VIII. They have similar power dissipation and area. For an 130 nm technology node the power dissipation of a SCB IFC circuit is almost the same as for a conventional analog IFC circuit. Scaling down the technology, the energy *per* pulse relation may not be the same. The input BW and amplitude is quite different for the two prototypes. This difference is due to topology (pulse timing, pulse delay t_d, integration type, RC integration *versus* load capacitor current integration), amplifier gain, and comparator thresholds. In fact, it can be seen that the SCB IFC average firing-rate is 66 times higher than the analog version, giving a much smaller minimum IPI for the SCB prototype than the analog IFC prototype. The SCB IFC presents minimum IPI values of approximately 0.2 μs *versus* 10 μs for the analog IFC for 1 kHz input signal, this also due to the fact that the input signal amplitude is much larger for the SCB IFC to have pulses. The SCB IFC presents some crossover distortion, as shown in [13], due to the minimalist inverter-based amplifier (class B amplifier) and open-loop configuration. Without feedback, the circuit does not force the input transistors to be always biased in the same biasing point. The analog IFC does not present crossover distortion. During measurement it was noticed that the SCB IFC is more stable, robust, and insensitive to parasitics than the analog IFC. Although, for the SCB IFC circuit the input CM has to be finely adjusted to the amplifier inverters mid point and is more sensitive to PVT variation [13], while the analog

TABLE VI
CONVERSION PLUS RECONSTRUCTION ERRORS

Signal & IFC	Sine in SCB	Sine in Analog	ECG in Analog
Type	Measured 14 mVp 1 kHz	Simulation 0.6 mVp 100 Hz	Simulation Acc. 100×
Fig.	12 (right)	13 (bottom left)	17 (right)
NMAE (%)	5.06	0.31	1.21
NRMSE (%)	0.26	1.19	5.18

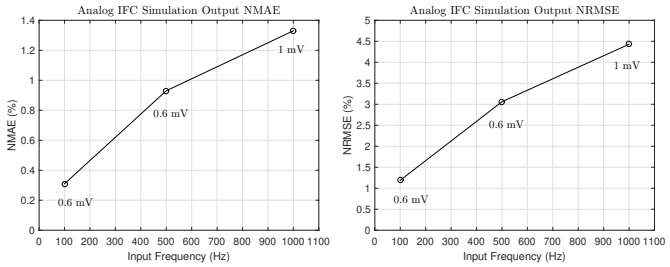

Fig. 18. Analog IFC Simulation output conversion plus reconstruction errors versus input signal frequency: NMAE (left), input peak amplitude in the data points label, and NRMSE (right).

TABLE VII
CONVERSION PLUS RECONSTRUCTION ERROR COMPARISON

Work	ISCAS JLPEA [40], [41]	JSSC [42]	**This Work Analog**	**This Work SCB [13]**
Application	Extrema Det.	LC-ADC	IFC	IFC
Platform	FPAA	ASIC	ASIC	ASIC
Tech. (nm)	350	40	130	130
Signal	ECG,Chirp	ENG	ECG,Sine	Sine
Input BW (Hz)	60, 1000	10000	10 - 4000	2 - 42000
Power (μW)	4.3, 12.3	50	53	59
NRMSE (%)	26.1, 4.4	4	5.18, 1.19	0.26

Table Acronyms: level-crossing (LC), field-programable analog array (FPAA), application-specific IC (ASIC), electroneurogram (ENG)

TABLE VIII
ANALOG AND SCB IFCS COMPARISON

IFC Version	Analog	SCB [13]
Supply (V)	0.9	0.9
Area (mm^2)	0.027	0.021
Total Power (μW)	53	59
Energy *per* Pulse (pJ)	1060	18
Average Firing-rate (kHz)	20 - 50	3.3×10^3
Input BW	10 Hz - 4 kHz	2 Hz - 42 kHz
Input Amplitude V_p (mV)	0.3 - 1.2	0.8 - 14
Input CM (mV)	400	435
Input Impedance Type	R	C
Minimum IPI (μs)	10	0.2
Fire Thresholds (mV)	500 +/− 100 $_{(a)}$	415 +/− 200 $_{(b)}$
IFC minimum ΔV_{th} (mV)	40 $_{(c)}$	-
Minimum comparator input difference (mV)	18 $_{(d)}$	22 $_{(e)}$

(a) Typical thresholds settings defined by the user. (b) Simulation measured fixed thresholds (typical corner simulation with R+C+CC extraction type), defined by the latch transistors dimensions. (c) Prototype measurement. (d) Simulation measured minimum input difference to trigger the comparator with $V_{thp} = V_{thn} = V_{oCM} = 500$ mV. (e) Simulation measured minimum input difference to trigger the SCB comparator.

TABLE IX
PROTOTYPE COMPARISON

Work	TCASI [23]	F.Neuro. [24]	TCASI [25]	NatureC. [22]	**This Work Analog**	**This Work SCB [13]**
Tech. (nm)	$22_{(a,b)}$	65	$28_{(b)}$	180	**130**	**130**
Supply (V)	0.8	0.2	0.2-1	1.8	**0.9**	**0.9**
Area (mm^2)	-	35×10^{-6}	13.3×10^{-6}	0.018	**0.027**	**0.021**
Power (μW)	-	1×10^{-4}	1.85×10^{-4}	27.3	**53**	**59**
Energy *per* Pulse (pJ)	1 @2.1 kHz	4×10^{-3}	0.43×10^{-3}	883 @30 Hz	**1060**	**18**
Avg. Firing-rate (kHz)	0.07	25	430	-	**20 - 50**	**3300**

(a) FDSOI (b) From simulation results, i.e., not prototyped.

IFC accepts a larger range of input CM, from approximately 0.35 V to 0.5 V. The SCB IFC circuit has a simpler design with less optimization and also higher dynamic range than the analog IFC circuit. The analog IFC circuit is more versatile than the SCB IFC circuit, as it is possible to change the firing thresholds and so the number of output pulses, which reflects in the reconstruction accuracy, or feature extraction capability, when doing pulse processing.

Table IX presents the prototypes comparison with the state-of-the-art. The proposed IFC is the first SCB and the only one that can be used standalone as an AFE in this comparison, together with the proposed analog IFC version. [19] and the two proposed IFCs are the only biphasic IFCs in this comparison. The presented power dissipation and average firing-rate are not for the same input signal conditions. The comparison should be done taking that in account. The average firing-rate approximation of 20 - 50 kHz for the proposed analog IFC was obtained for input signals with frequency and peak amplitude of 100 Hz and 600 μV, Fig. 14, to 1 kHz and 1 mV, respectively. The average firing-rate approximation of 3300 kHz for the proposed SCB IFC was obtained for an input signal with frequency of 1 kHz and 14 mV peak amplitude, Fig. 12. This way, for a fairer comparison the energy *per* pulse consumption was calculated for each prototype. The energy *per* pulse was calculated for the presented average firing-rate, or stated otherwise in Table IX, considering $Energy-per-Pulse = \frac{Power}{Avg.\ Firing-rate}$. The energy *per* pulse scales significantly with process node, [32, p. 72]. As the protoypes were fabricated in an 130 nm tech node, the presented energies *per* pulse could be further reduced, if prototyped in smaller nodes as 65 nm, 28 nm, and 22 nm, or even with more recent FinFET or Gate All Around technologies. The work [23] in Table VIII presents a low energy *per* pulse, but uses an FDSOI process that has 2 V back gate bias to reduce the overall power consumption. This implies the use of one more power supply, or a voltage doubler to generate this voltage on chip. The proposed IFCs only need a simple power supply and a few voltage regulators present in the protoyped PCB. These intermediate voltages could be easily generated on chip. Also, FDSOI technology has not become a main trend in semiconductor industry. The main ones are FinFET and Gate All Around technologies and these do not allow the use of a back gate voltage. So the work [23] may not achieve so low power dissipation when scaled to more recent technologies. Considering the example in [32, p. 72] work, the estimated reduction in energy consumption for the proposed analog and the SCB IFCs with scaling to 12 nm technology node, for example, would probably not be enough to be more energy efficient than the works presented in [24] and [25]. Although, in the case of the SCB IFC, as it is SCB, the energy consumption reduction would probably be higher than in the proposed analog IFC.

V. CONCLUSION

A pseudo-differential voltage mode SCB IFC circuit is presented in this paper, together with a fully differential voltage mode IFC circuit, both with 0.9 V supply. They were prototyped in a 1.2 V 130 nm CMOS standard process. The SCB occupies an area of 0.021 mm^2 and the analog version 0.027 mm^2, they are both the first of their kind. A comparison between the proposed analog IFC and SCB IFC [13] circuits is presented in this paper. The SCB IFC is fully digital, dynamic, and synthesizable. The two can be used as AFEs in sensor-to-digital interfaces. They have a total power dissipation of 59 μW and 53 μW, and an energy *per* pulse consumption of 18 pJ and 1060 pJ, SCB and analog version, respectively.

The SCB energy *per* pulse consumption of 18 pJ is one of the lowest energy *per* pulse consumption reported for IFC circuits. They present interesting characteristics to be applied in ECG and neural signals, provided that a good AFE is used before the IFC circuit, in the latter case (because of minimum detectable signal constraints). It represents a low power solution with low output data rates that can be considered for biological implantation, or as an AFE for low frequency signals, as required in IoT. The future work will focus on time domain feature extraction, using these IFCs.

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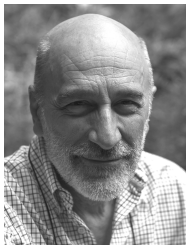

José C. Príncipe (M'83–SM'90–LF'00) received the Ph.D. degree in electrical and computer engineering from the University of Florida, Gainesville, FL, USA, in 1979. He is currently a Distinguished Professor of electrical and computer engineering with the University of Florida, where he is also the Don D. and Ruth S. Eckis Chair with the Department of Electrical and Computer Engineering and the Department of Biomedical Engineering. He is the Founding Director of the Computational NeuroEngineering Laboratory, University of Florida. His current research interests include advanced signal processing and machine learning, brain machine interfaces, and the modeling and applications of cognitive systems.

João Goes (S'95–M'00–SM'09) graduated from Instituto Superior Técnico (IST), Lisbon, in Electrical and Computer Engineering (ECE), in 1992. He obtained the M.Sc. and the Ph.D. degrees in ECE, respectively, in 1996 and 2000, from the Technical University of Lisbon and the 'Habilitation' degree, in Electronics, in 2012 from the NOVA University of Lisbon (NOVA). Since 1998 João Goes has been with the Department of Electrical and Computer Engineering (DEEC) of the School of Sciences and Technology of NOVA where he is a Full Professor.

From 2012 till 2019 He headed the DEEC, comprising 50 professors and over 1000 students. From 2012 to 2017, he was the Director of the Centre of Technology and Systems (CTS) of the Research Institute for New Technologies (UNINOVA), leading nearly 50 Senior Researchers with a PhD, over 70 collaborators and more than 90 PhD students. Since Jan. 2023 he is the Executive Director of UNINOVA. He has been elected a member of the Scientific Council of FCT NOVA for 12 years, and he has been elected a member of the General Council of NOVA, the top governing body of the University, for the 2022-2025 term.

In 2003 he co-founded and served as CTO of ACACIA Semi. SA, a Portuguese engineering company specialized in high-performance analog front-end products (now RENESAS). From 1997 until 1998 João was Project Manager at CHIPIDEA SA (now SYNOPSYS). He was the first Engineer hired. From 1993 to 1997 he worked as a Researcher at Integrated Circuits and Systems Group (GCSI) at IST doing research on data converters and filters. Since 1992 he has participated and led several National and European projects in science, technology, networking, and training. He has been the Primary Investigator of over 20 projects.

João Goes has published over 200 papers in international journals (50+) and IEEE leading conferences, he holds 4 international patents, and he is co-author of 8 books. He was Associate Editor (AE) of IEEE Transactions on Circuits and Systems–II, for the period 2016-2023 and he is (2024 -) AE of IEEE Transactions on Circuits and Systems–I. He was the Chairman of the IEEE CASS Analog Signal Processing Technical Committee, for the term 2013-2015. Among several best-paper awards, he is co-author of the journal paper recipient (winner) of the 2012 IEEE CASS Outstanding Young Author Award and co-winner (1st place) of the first edition of the "Innovation Award INCM" in 2016.